

CLAIMS

1. (Currently Amended) A type of solid-state image sensing device characterized by the fact that the solid-state image sensing device is comprising an integration of plural pixels, each of which has a light-receiving portion that receives light and generates and accumulates a signal charge, and has the following parts:

a semiconductor substrate of the first electroconductive type;

a semiconductor layer of the second electroconductive type that is formed on the principal surface of said semiconductor substrate;

a gate electrode for pixel selection formed via a gate insulating film on said semiconductor layer;

a first semiconductor region of the first electroconductive type that is formed in the outer layer of said semiconductor layer in the light-receiving portion positioned on one side of said gate electrode for pixel selection;

a second semiconductor region of the first electroconductive type formed deeper than said first semiconductor region in the outer layer of said semiconductor layer in said light-receiving portion;

and a third semiconductor region of the first electroconductive type formed in the outer layer of said semiconductor layer on the other side of the gate electrode for pixel selection, and containing an impurity of the first electroconductive type and having an impurity concentration higher than that of said first semiconductor region.

2. (Currently Amended) The solid-state image sensing device described in Claim 1 characterized by the following facts wherein:

in said semiconductor layer of said light-receiving portion, light is received and the generated signal charge is accumulated;

in said light-receiving portion, modulation of the threshold of the junction transistor comprising said semiconductor substrate, said semiconductor layer, and said second semiconductor region is performed by means of the signal charge accumulated in said semiconductor layer.

3. (Currently Amended) The solid-state image sensing device described in Claim 1 characterized by the following facts further comprising:

[it also has] a gate electrode for reset that is formed via a gate insulating film on said semiconductor layer, and

a fourth semiconductor region of the second electroconductive type that is formed in the outer layer of said semiconductor layer on one side of said gate electrode for reset;

said first semiconductor region is formed in the outer layer of said semiconductor layer on the other side of said gate electrode for reset;

said semiconductor layer, said gate electrode for reset, and said fourth semiconductor region form a buried-channel type of transistor for reset, and said signal charge accumulated in said light-receiving portion is evacuated from said light-receiving portion when said transistor for reset operates.,

4. (Currently Amended) The solid-state image sensing device described in Claim 3 characterized by the fact that wherein

said gate electrode for pixel selection in one pixel is connected to said gate electrode for reset in the pixel adjacent to said one pixel.

5. (Currently Amended) The solid-state image sensing device described in Claim 3 characterized by the fact that further comprising

a fifth semiconductor region of the first electroconductive type, having an impurity of the first electroconductive type and having an impurity concentration higher than that of said first semiconductor region, is formed in the outer layer of said semiconductor layer on the periphery of said first semiconductor region and in the portion other than the portion where said gate electrode for pixel selection and said gate electrode for reset are located.

6. (Currently Amended) The solid-state image sensing device described in Claim 5 characterized by the fact that further comprising

a field plate [[is]] formed, as the gate electrode of a transistor for element separation, via a gate insulating film in the upper layer of the semiconductor layer between adjacent pixels on the outer periphery of said fifth semiconductor region.

7. (Currently Amended) A type of solid-state image sensing device characterized by the following facts: comprising:

the solid-state image sensing device has plural pixel rows formed from plural light-receiving elements arranged in a linear configuration, with light-receiving elements in each pixel row arranged offset by about 1/2 pitch from those in the adjacent rows;

each said light-receiving element has the following parts:

a semiconductor layer of a first electroconductive type formed on the principal surface of a semiconductor substrate;

a gate electrode for read formed via an insulating film on said semiconductor layer on one side of the pixel row;

a gate electrode for reset formed via an insulating film on said semiconductor layer on the other side of the pixel row;

a first semiconductor region of the second electroconductive type formed in the region between said gate electrode for read and said gate electrode for reset;

a second semiconductor region of the second electroconductive type, having an impurity concentration higher than that of said first semiconductor region and formed on said semiconductor layer in a region nearer said gate electrode for read than said gate electrode for reset in said first semiconductor region;

a third semiconductor region of the second electroconductive type, having an impurity concentration higher than that of said first semiconductor region and formed on said semiconductor layer in the region facing said first semiconductor region with said gate electrode for read sandwiched between them;

and a fourth semiconductor region of the first electroconductive type, having an impurity concentration higher than that of said semiconductor layer and formed on said semiconductor layer in the region facing said first semiconductor region with said gate electrode for reset sandwiched between them;

said gate electrodes for read and gate electrodes for reset of the facing light-receiving elements in adjacent pixel rows are electrically connected to each other.

8. (Currently Amended) The solid-state image sensing device described in Claim 7 characterized by the fact that wherein

said gate electrodes for read and said gate electrodes for reset of the facing light-receiving elements in the adjacent pixel rows are formed by a single electroconductive layer, and said electroconductive layer is arranged to zigzag between the adjacent pixel rows.

9. (Currently Amended) The solid-state image sensing device described in Claim 7 or 8 characterized by the fact that wherein

said first semiconductor regions of the light-receiving elements in the same pixel row are separated from each other by a fifth semiconductor region of the second electroconductive type that has an impurity concentration higher than said that of first semiconductor region.

10. (Currently Amended) The solid-state image sensing device described in Claim 9 characterized by the fact that further comprising

a plate electrode [is] formed via an insulating film on said fifth semiconductor region.

11. (Currently Amended) The solid-state image sensing device described in Claim 7, 8, 9 or 10 characterized by the fact that wherein

when a first voltage is applied to said gate electrode for reset, said light-receiving element is reset and the charge accumulated in said light-receiving element is evacuated, and when a second voltage is applied to said gate electrode for read, a signal corresponding to the charge accumulated in said light-receiving element is output.

12. (Currently Amended) The solid-state image sensing device described in Claim 7, 8, 9, 10 or 11 characterized by the fact that wherein

said first, second and third semiconductor regions have p-type electroconductivity, while said semiconductor layer and said fourth semiconductor region have n-type electroconductivity.

13. (New) The solid-state image sensing device described in Claim 8 wherein said first semiconductor regions of the light-receiving elements in the same pixel row are separated from each other by a fifth semiconductor region of the second electroconductive type that has an impurity concentration higher than said that of first semiconductor region.

14. (New) The solid-state image sensing device described in Claim 8 further comprising

a plate electrode formed via an insulating film on said fifth semiconductor region.

15. (New) The solid-state image sensing device described in Claim 8 wherein when a first voltage is applied to said gate electrode for reset, said light-receiving element is reset and the charge accumulated in said light-receiving element is evacuated, and when a second voltage is applied to said gate electrode for read, a signal corresponding to the charge accumulated in said light-receiving element is output.

16. (New) The solid-state image sensing device described in Claim 9 wherein when a first voltage is applied to said gate electrode for reset, said light-receiving element is reset and the charge accumulated in said light-receiving element is evacuated, and when a second voltage is applied to said gate electrode for read, a signal corresponding to the charge accumulated in said light-receiving element is output.

17. (New) The solid-state image sensing device described in Claim 10 wherein when a first voltage is applied to said gate electrode for reset, said light-receiving element is reset and the charge accumulated in said light-receiving element is evacuated, and when a second voltage is applied to said gate electrode for read, a signal corresponding to the charge accumulated in said light-receiving element is output.

18. (New) The solid-state image sensing device described in Claim 8 wherein said first, second and third semiconductor regions have p-type electroconductivity, while said semiconductor layer and said fourth semiconductor region have n-type electroconductivity.

19. (New) The solid-state image sensing device described in Claim 9 wherein said first, second and third semiconductor regions have p-type electroconductivity, while said semiconductor layer and said fourth semiconductor region have n-type electroconductivity.

20. (New) The solid-state image sensing device described in Claim 10 wherein said first, second and third semiconductor regions have p-type electroconductivity, while said semiconductor layer and said fourth semiconductor region have n-type electroconductivity.